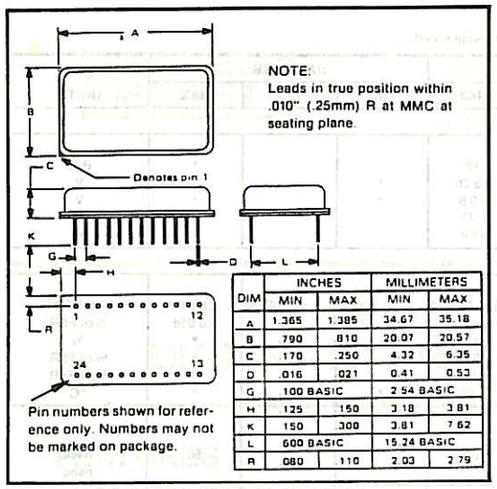
MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

PIN ASSIGNMENTS

Pin	Function	Pin	Function
1	Bit 1 (MSB, Data Input)	14	Digital Common (V_{DD} Common)
2	Bit 2	15	Analog Common ($\pm V_{CC}$ Common)
3	Bit 3	16	Analog Common
4	Bit 4	17	Analog Common
5	Bit 5	18	Analog Common
6	Bit 6	19	V_{DD} (Logic Supply)
7	Bit 7	20	I_{OUT} (Current Output)
8	Bit 8	21	R_f (Application Resistor)
9	Bit 9	22	BPO (Bipolar Offset)
10	Bit 10	23	$-V_{CC}$ (Negative Analog Supply)
11	Bit 11	24	$+V_{CC}$ (Positive Analog Supply)
12	Bit 12 (LSB)		
13	No connection		

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC812 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB (±1LSB for the BM model) from a best-fit straight line over the specified temperature range of −25°C to +85°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a −25°C to +85°C range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by 1) testing the end point differences for the DAC812 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around the minus full-scale point over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC812 is ±4.0V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC812 (pins 14, 15, 16, 17, and 18). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC812. To achieve fast settling performance it is recommended that pins 14 through 18 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC812 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

SETTLING TIME

Settling time for the DAC812 is the total time required for the output to settle within an error band around its

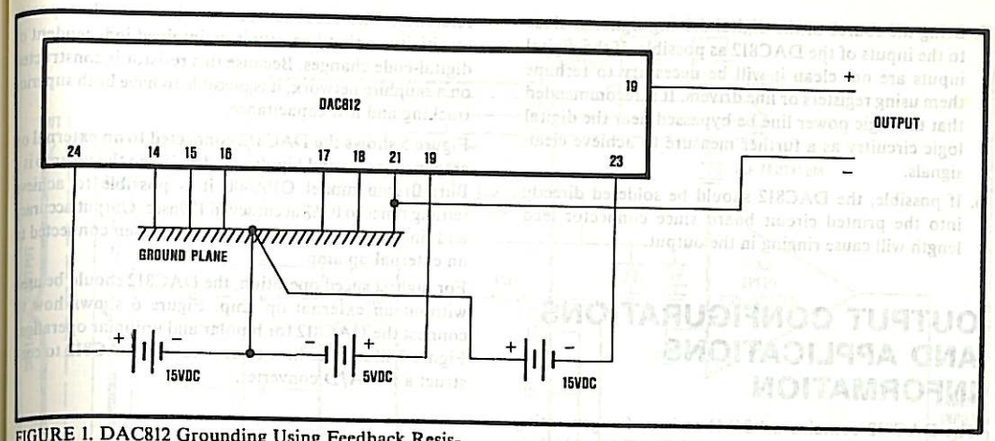


FIGURE 1. DAC812 Grounding Using Feedback Resistor to Generate Output Voltage.

final value after a digital input change. This time includes the digital delay of the internal switches.

Figure 2 shows a typical settling time curve of the DAC812 versus output error. This curve is for full-scale digital code changes. Figures 3 and 4 show typical measured settling time characteristics of the DAC812.

In order to achieve the minimum settling time, it is necessary to observe the following good high frequency construction techniques.

1. The power supplies should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Keep analog and digital signal lines physically separated to avoid coupling of the digital signal into the analog paths.

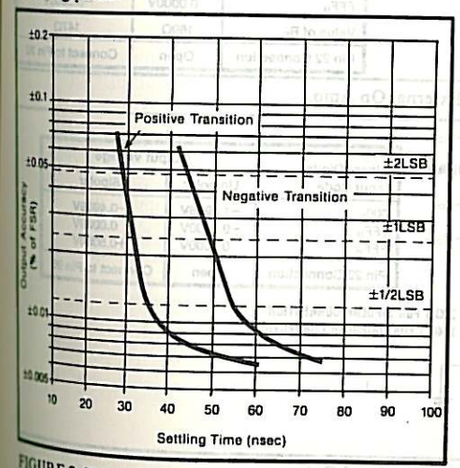


FIGURE 2. DAC812 Typical Settling Time vs. Accuracy

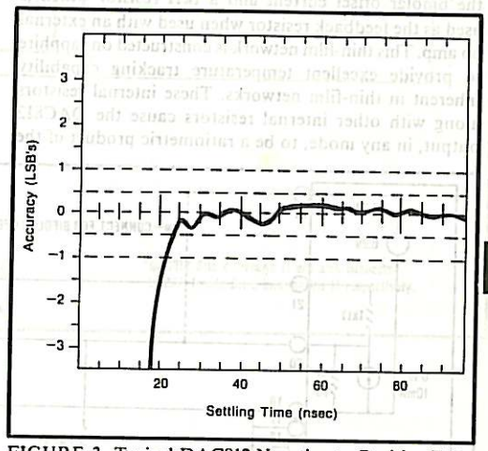


FIGURE 3. Typical DAC812 Negative-to-Positive Full-Scale Output Characteristic.

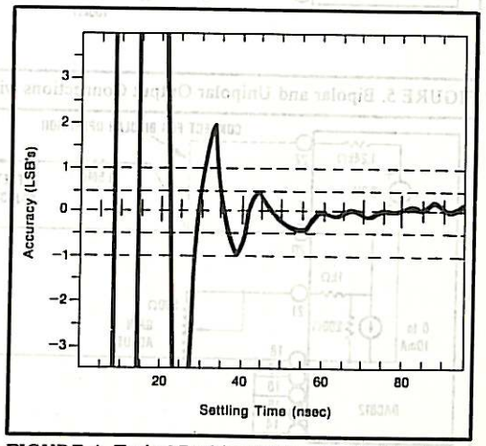


FIGURE 4. Typical Positive-to-Negative Full-Scale Output Characteristic.